REMARKS

In response to the Office Action dated December 20, 2007, claims 5, 7, 8 and 11 are amended, claims 12 and 13 are cancelled without prejudice, and claims 21-22 are newly added. Claims 1-4, 9-10, and 14-20 were previously cancelled without prejudice. Claims 5-8, 11 and 21-22 are now active in this application. No new matter has been added. Claims 11 is the only independent claim.

Claim 13 was rejected under 35 U.S.C. § 112, first paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Applicants submit that this rejection is moot because claim 13 has been cancelled.

Claims 5-7 and 11-12 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Arimoto et al. (U.S. 2003/0090449) in view of Kanauchi et al. (U.S. 6,788,277). Applicants traverse this rejection.

Claims 8 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Arimoto in view of Kanauchi, and further in view of Park (U.S. 2002/0084959). Applicants traverse this rejection.

Independent claim 11 recites, in part:

> the control circuit outputs a first clock signal and the display data to the data driver;
> the control circuit outputs to the scan driver a second clock signal, the second clock signal synchronized with the first clock signal and providing a two clock period at every n signal creation, by way of not being created every n (n>2) signal creation thereof and outputs a scanning start signal generated a plurality of times during one frame period; and
> **the control circuit outputs to the data driver blanking data other than the display data in place of the display data during one clock**

signal period in the first half of the two clock signal period at every n signal creation;

the data driver, in accordance with the first clock signal, sequentially supplies tone voltage corresponding to the display data received from the control circuit and tone voltage in accordance with the blanking data received in place of the display data from the control circuit, to the pixels;

the scan driver, in accordance with the second clock signal, sequentially shifts pixel rows to be selected, and during one clock signal period in the first half of the two clock signal at every n signal creation, in addition to pixel rows being sequentially shifted, for selecting the other plurality of pixel rows separated from the pixel rows being sequentially shifted by a plurality of rows; and

the scan driver, in accordance with the scanning start signal, further repeats selecting operation of the pixel rows sequentially shifted in accordance with the second clock signal and selecting operation of the other plurality of pixel rows.

As an illustrative and non-limiting example of claim 11, FIGS. 7 and 8 of the present application insert BK data (black data) during one clock signal period, (one clock signal period in the first half of the two clock signal period) which is just before the CL3 signal is not generated, supplying tone in accordance with BK data to a pixel row through data driver 103. The scan driver during one clock signal period (one clock signal period in the first half of the two clock signal period) selects pixels row G257 to G268 which are different from sequentially shifted pixel rows G1 to G12. Thus, display data is displayed at sequentially shifted pixel rows G1 to G12, and BK data is displayed at pixel rows G257 to G268.

Additionally, as shown in FIGS. 7 and 8, double gate driving is realized with an FLM signal by repeating twice the selecting operation of pixel rows by scan driver 104 in accordance with the CL3 signal.

In order to establish *prima facie* obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. Further, "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of

obviousness." *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006). At a minimum, the cited prior art references do not disclose (expressly or inherently) or suggest the above recited highlighted (bolded) elements regarding control circuit outputs and scan driver outputs.

The Office Action, at pages 4 and 5, asserts that all of the elements of claim 11 are allegedly disclosed by the combination of Arimoto and Kanauchi.

Specifically, the Office Action asserts that FIG. 9 of Arimoto allegedly discloses the control circuit output elements of claim 11, with specific reference to elements 902 and 401 shown in that drawing. However, FIG. 9 of Arimoto is described at paragraphs [0115] to [0118], which merely state:

> [0115] FIG. 9 is a block diagram showing the construction of a liquid crystal device according to a first embodiment of the present invention. In FIG. 9, the liquid crystal display device includes a signal converting unit 401, a driving pulse generating section 902, a source driver 403, a gate driver 404, and a liquid crystal panel 405. Note that the first embodiment is different from the virtual example illustrated in FIG. 4 only in the driving pulse generating section. In FIG. 9, the components equivalent to those illustrated in FIG. 4 are provided with the same reference numerals, and are not described herein. The driving pulse generating section 902 generates pulses for driving the respective drivers 403 and 404. To facilitate understanding of the description, assume for convenience sake that the number of source lines of the liquid crystal panel 405 is ten (SL1 to SL10), the number of gate lines is ten (GL1 to GL10), and one frame period is composed of ten horizontal periods.
> [0116] Described next is an operation of anti-back transition to be carried out by the liquid crystal device according to the first embodiment. An input image signal is doubled in speed line by line in the signal converting section 401, and is then supplied to the source driver 403.
> [0117] The specific construction of the signal converting section 401 and the timing of the converting operation have been described in the description of the virtual example with reference to FIG. 5 and FIG. 6, and are therefore not described herein. From the signal converting section 401, a non-image signal and an image signal that have been doubled in speed line by line are outputted in time sequence during one horizontal period of the input signal.
> [0118] The source driver 403 alternately inverts the signal (double-speed signal) outputted from the signal converting section 401 for supply to the source lines (SL1 to SL10) of the liquid crystal panel 405.

In other words, Arimoto is directed to merely improving insufficient writing, and the Arimoto device is structured for writing an image signal with the same polarity during just before a normal writing period of the image signal. This is known as "pre-charge driving." Further, Arimoto merely writes a non-image signal at each of the four lines, as illustrated in FIG. 6. Further, Arimoto merely discloses selecting two gates at the same time in FIG. 26, but does not disclose by what kind of signal the two gates are selected simultaneously.

Thus, Arimoto does not teach or suggest "**the control circuit outputs to the data driver blanking data other than the display data in place of the display data during one clock signal period in the first half of the two clock signal period at every n signal creation,**" and does not teach or suggest, "**the scan driver, in accordance with the second clock signal, sequentially shifts pixel rows to be selected, and during one clock signal period in the first half of the two clock signal at every n signal creation, in addition to pixel rows being sequentially shifted, for selecting the other plurality of pixel rows separated from the pixel rows being sequentially shifted by a plurality of rows,**" as required by claim 11.

Further, the Office Action refers to FIG. 14 of Kanauchi, which is described at column 11, lines 14-44, which merely state:

> Then, when black display regions in an erase gate output stage status (j) shown in FIG. 14 are scanned, the erase TFTs (Tr.sub.3) described above are turned on. Thus, the data of the video signal (d) remaining in the latch circuit 1.sub.b in the display region 1 is ignored, and the light-emitting elements corresponding to the pixels of the non-display regions are placed in a forcibly extinguished state. Further, when the region of a display 2 is scanned, the image based on the video signal (d) is displayed on the display region 2 in FIG. 12.
> Then, in this embodiment, the supply of the scan clock signal (e) is stopped as shown in FIG. 14 at the time the scan of the display region 2 has been completed. That is, when the supply of the scan clock signal (e) is stopped, data remains in the shift resister 2.sub.a of the first scan driver 2. However, since the erase gate output stage status (j) described above is displayed in black in the region under the display region 2, the light-emitting elements corresponding to the region are entirely extinguished.

According to the second embodiment described above, it is possible to obtain an operation/working-effect similar to the first embodiment described above as well as it is possible to stop the scan clock signal when the end of the display region of the one frame (one sub-frame) is reached as shown in FIG. 14(e). With this operation, lower power consumption can be realized. Moreover, according to this embodiment, the partial display described above can be realized without the addition of a circuit for resetting the shift resister in the scan driver as in the conventional example, thereby the problem of a decrease in the opening ratio can be avoided.

Thus, Kanauchi does not teach or suggest "**the control circuit outputs to the data driver blanking data other than the display data in place of the display data during one clock signal period in the first half of the two clock signal period at every n signal creation,**" and does not teach or suggest, "**the scan driver, in accordance with the second clock signal, sequentially shifts pixel rows to be selected, and during one clock signal period in the first half of the two clock signal at every n signal creation, in addition to pixel rows being sequentially shifted, for selecting the other plurality of pixel rows separated from the pixel rows being sequentially shifted by a plurality of rows,**" as required by claim 11.

Thus, at a minimum, the combination of Arimoto and Kanauchi fails to teach or suggest the forgoing elements, and therefore claim 11 is allowable over the cited art.

The other cited art, Park, does not remedy the deficiencies of Arimoto and Kanauchi.

Further, Applicants submit that dependent claims 5-8, 21, and 22 are allowable over the cited art for similar reasons to claim 1.

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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